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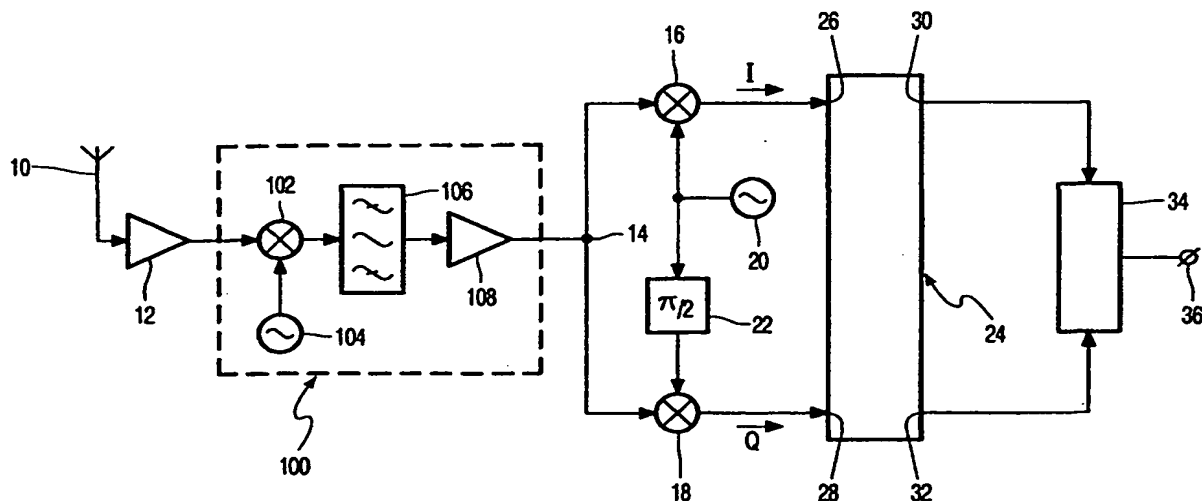
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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).			
(71) Applicant (for SE only): PHILIPS AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE).			
(72) Inventors: MOORE, Paul, Anthony; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DAVIE, Alan, James; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).			
(74) Agent: MOODY, Colin, J.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).			

(54) Title: IMPROVEMENTS IN OR RELATING TO PHASING RECEIVERS



(57) Abstract

A phasing receiver comprises mixing means (16, 18, 20, 22) for frequency converting an input signal to quadrature related low IF signals (I, Q). The low IF signals are applied to a polyphase filter (24) which functions as a low pass and an adjacent channel rejection filter. Means (Figures 3 to 5 - not shown) for fine adjustment of the phase and/or amplitude of the input signals are provided for improving the image rejection due to mismatches in an input stage of the polyphase filter (24).

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DESCRIPTION

IMPROVEMENTS IN OR RELATING TO PHASING RECEIVERS

5 Technical Field

The present invention relates to phasing receivers and particularly, but not exclusively to polyphase or sequence - asymmetric receivers which may be implemented as an integrated circuit.

10 Background Art

A popular type of architecture for use as an integrated receiver is a zero - IF architecture in which an input signal is frequency downconverted to a zero - IF using quadrature mixers, the wanted signals are selected from the products of mixing using low pass filters and the wanted signals are processed further
15 to provide a demodulated output.

Most of the limitations which beset the zero - IF receiver arise either directly or indirectly from the fact that components of wanted signals translated down to IF frequencies at or around DC cannot be distinguished from components of unwanted signals which appear in the same frequency range
20 as a result of inherent circuit deficiencies.

The above - mentioned limitations in a zero - IF receiver may be eliminated substantially in a low - IF superheterodyne receiver but this would suffer from an image response that could not be eliminated by realistic front-end filters.

25 Another receiver architecture termed a phasing receiver, is a low - IF receiver based on the principle of the image - reject mixer in which the image response is removed by cancellation, rather than filtering, but the level of image rejection which can be achieved, even in fully - integrated form, is severely limited by the degree of matching which can be obtained between nominally
30 identical components. A particular example of a phasing receiver is the polyphase or sequence - asymmetric receiver in which the conventional IF

filters, IF phase shifters and IF signal combiner are replaced by a single polyphase IF filter. This very substantially increases the level of image rejection which can be obtained. In spite of the increased level of image rejection there may still a need to improve further the level of image rejection.

5

Disclosure of Invention

An object of the present invention is to improve the image rejection capability of a phasing receiver.

According to one aspect of the present invention there is provided a
10 phasing receiver having a polyphase or sequence - asymmetric gyrator filter in which lack of image rejection is improved by the fine adjustment of the phase and/or amplitude of input signals.

According to a second aspect of the present invention there is provided a phasing receiver comprising an input, first and second signal mixing means
15 for providing quadrature related low IF frequencies, a polyphase filter having inputs coupled to outputs of the first and second signal mixing means and signal demodulating means coupled to outputs of the polyphase filter, and means for effecting fine adjustment of the phase and/or amplitude of signals applied to the inputs of the polyphase filter to compensate for less than
20 optimum image rejection.

By means of the present invention fine adjustment of the amplitude and/or phase of the pair of IF signals feeding a polyphase IF filter can further improve the level of image rejection which can be obtained, typically by at least 10dB.

25

Brief Description of Drawings

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a block schematic diagram of a polyphase receiver,

30 Figure 2 is a simplified circuit diagram of a current - fed polyphase or sequence - asymmetric gyrator filter,

Figures 3A and 3B show one arrangement by which amplitude may be adjusted,

Figures 4A and 4B show another arrangement by which amplitude may be adjusted,

5 Figure 5 shows one arrangement by which phase may be adjusted, and

Figures 6 to 13 are graphs showing the lack of image rejection due to errors in the resistance R3, the capacitance C6 and the cross coupling gyrator JC17, shown in Figure 2.

10 In the drawings the same reference numerals have been used to indicate corresponding features.

Modes for Carrying Out the Invention

Referring to Figure 1, the illustrated polyphase receiver comprises a low IF receiver in which the local oscillator frequency is offset by, for example, half
15 the channel bandwidth from the nominal carrier frequency of an input signal received by an antenna 10.

Ignoring the components in the box 100, the antenna 10 is coupled by an RF amplifier 12 to a signal splitter junction 14. First and second mixers 16, 18 each have a first input coupled to the junction 14. A local oscillator 20 is
20 coupled to the second input of the first mixer 16 and, by way of a 90 degree phase shifter 22, to a second input of the second mixer 18. The in-phase products I of mixing present at an output of the first mixer 16 are applied to a first input 26 of a current-fed polyphase filter 24. The quadrature phase products Q of mixing present at an output of the second mixer are applied to
25 a second input 28 of the filter 24.

The polyphase filter 24 functions as an image rejection filter and a channel selectivity filter. Outputs 30, 32 of the filter 24 are coupled to a demodulator 34 having an output terminal 36.

Referring to the components in the box 100, the signal from the RF
30 amplifier 12 is applied to a superhet frequency down conversion stage comprising a mixer 102 to which an output from a local oscillator 104 is

applied. A bandpass filter 106 selects an IF signal which is amplified in an IF amplifier 108 and supplied to the junction 14. Thus the quadrature frequency down conversion stage operates on the IF signal instead of the RF signal which will be the case if the superhet stage is not present. For convenience of description it will be assumed that the superhet stage is not present.

Although the polyphase filter 24 has been identified as being current fed, it may be voltage fed depending on the application.

Figure 2 illustrates an embodiment of a 5th order polyphase filter 24. The filter comprises 2 sets of stages, corresponding stages in each set being identical. For convenience of description only one set of the stages will be described and the corresponding components in the non-described set will be shown in parenthesis. A first stage of the filter comprises a source resistor R1 (R3), a capacitor C1 (C6) and a transconductor JC1 (JC9) are coupled in parallel between signal rails 38, 40. A cross-coupled gyrator consisting transconductors JC26 and JC17 is coupled to the signal rails 38, 40. A current source J1 (J2) representing the inputs is coupled to the signal rails 38, 40. The current sources J1, J2 correspond to inputs 26, 28, respectively, in Figure 1.

The second, third and fourth stages are of identical layout and will be described collectively. A transconductor JC2 (JC10), JC4 (JC12), JC6 (JC14) is connected in parallel with a capacitance C2 (C7), C3 (C8), C4 (C9) and another transconductor JC3 (JC11), JC5 (JC13), JC7 (JC15) between signal rails 42, 44. Cross coupled gyrators JC19 (JC18), JC21 (JC20) and JC23 (JC22) are coupled to the signal rails 42, 44 of the respective stages. The fifth stage of the filter comprises a transconductor JC8 (JC16), capacitance C5 (C10) and resistor R2 (R4) connected in parallel between signal lines 46, 48. A cross coupled gyrator JC25 (JC24) is coupled to the signal rails 46, 48. Outputs 30, 32 are derived from the fifth stages.

The response of the polyphase filter 24 is centred on the low IF frequency, for example 12.5kHz in the case of 25kHz channel spacing. The component values can be determined by a number of known techniques and reference may be made to "Handbook of Filter Synthesis" by Anatol I. Zverev,

published by John Wiley and Sons Inc., June 1967. Once the values of the resistors R2, R2, R3 and R4 and the transconductances of the transconductors JC1 to JC16 have been set the capacitances C1 to C5 (C6 to C10) determine the shape of the filter response and the filter bandwidth. The centre frequency
5 of the filter, in this example 12.5kHz, is determined by the cross-coupling gyrators JC17 to JC26 as discussed by J.O. Voorman, "The Gyrator as a Monolithic Circuit in Electronic Systems" PhD Thesis of Catholic University of Nijmegen, The Netherlands, 16 June 1977, pages 91 to 103.

A polyphase filter is normally fabricated as an integrated circuit and if the
10 components were truly identical, the response would be a perfect as can be designed. However due to limited matching capabilities of the components, image rejection by the polyphase filter will be less than perfect.

The present invention endeavours to reduce, if not remove, the mismatches in component values by predistorting the amplitude and/or phase
15 of drive signals in order to correct for the frequency dependent errors produced by the mismatches.

An examination of the effects of these mismatches has shown that mismatches between components in the early stages, especially the first stage, are responsible for the degrading of the image rejection. However because
20 these components are in the early stages, the errors which they produce do not vary rapidly across the bandwidth of the filter. It has been found that it is possible to substantially correct for these errors by means of an essentially constant phase and/or amplitude correction inserted in the RF signal path, the local oscillator signal path or the low IF path. If the superhet stage is present,
25 the correction would be in the higher IF path, the local oscillator signal path or the low IF path.

Referring to Figure 2, the mismatches are considered are those between (a) the source resistors R1 and R3, (b) the first capacitors C1 and C6, (c) the amplitude match of the forward and reverse paths of the first cross-coupling
30 gyrator JC17, and (d) the phase match of the forward and reverse paths of the first cross-coupling gyrator JC17. Mismatch due to (a) above can be reduced

by fine adjustment of the phase of the IF input signals. The mismatch due to (b) above can be reduced by fine adjustment of the amplitude of the IF signals. The mismatch due to (c) above can be reduced by fine adjustment of the amplitude of the IF input signals and lastly the mismatch due to (d) above can be reduced by fine adjustment of the phase of the IF input signals.

Referring to Figure 1, the adjustment of the amplitude and/or phase of the IF input signals can be effected in the RF signal path to the first and second mixers 16, 18, for example at the junction 14. Also phase adjustment can be effected in the output path of the local oscillator 20 but it is not considered viable to make amplitude adjustments because the mixers 16, 18 are normally intentionally overdriven by the local oscillator 20. Amplitude adjustments may also be effected in the low IF signal paths between the outputs of the mixers 16, 18 and the filter inputs 26, 28, respectively. Although phase adjustments are theoretically possible in these latter signal paths, in reality they are impractical.

Figures 3A and 3B illustrate a method of effecting an amplitude adjustment in an analogue manner. Figure 3A shows a fixed potentiometer comprising resistors R1, R2 connected in series across an input of one of the signal paths and a junction 50 of these resistors being connected to an output. Figure 3B shows a variable potentiometer comprising a resistive potentiometer VR1 connected in series with a fixed resistor R3. An output is taken from the wiper of the potentiometer VR1. The values of the potentiometer VR1 and the resistor R3 can be determined statistically to introduce a sufficient adjustment range. The values of the resistors R1, R2 are then chosen to achieve the same attenuation as VR1 and R3, when the potentiometer VR1 is in its mid position. The potentiometer VR1 permits adjustments of the amplitude error to be made in each individual receiver to maximise image rejection.

The amplitude adjustment arrangement shown in Figures 4A and 4B differs from that shown in Figures 3A and 3B by a digitally controlled potentiometer VR2 being used in place of the combination of the potentiometer VR1 and the fixed resistor R3. The digital value is determined by measuring

image rejection and adjusting the attenuation to maximise the image rejection.

Figure 5 illustrates an arrangement for adjusting phase. In one of the signal paths an adjustable nominal 45 degree phase lead network PA1 is provided and in the other of the signal paths an adjustable nominal 45 degree phase lag circuit PA2 is provided. The circuits PA1 and PA2 each comprise a varactor diode VAD and a fixed resistor R4. Phase adjustment is effected by altering the capacitance value of the respective varactor diodes VAD. This can be effected digitally in which a stored digital value is applied to a digital to analogue converter DAC which supplies an analogue signal to a controller 52. The controller 52 produces control voltages VC_i and VC_o to adjust the varicap values electronically in the same direction. Although Figure 5 indicates a nominal relative phase difference of 90 degrees, this can be varied to give a smaller or greater phase difference depending on the respective phase mismatch in the receiver.

In practice it has been found that mismatches between capacitances C1 and C6 are corrected by adjustments in amplitude whereas mismatches between source resistors are corrected by phase adjustments. In other words the amplitude and phase adjustments act in an essentially orthogonal manner which enables each adjustment to be carried out substantially independently of the other.

Figures 6 to 13 are graphs which illustrate the effects of mismatches and the improvements obtainable by making the adjustments discussed. All the graphs are plots of frequency in Hz against the output across the resistor R2 in dBA. They all show a frequency shift of 300kHz and a -3dB bandwidth of 80kHz.

In Figures 6 to 13, the graphs have been folded about zero frequency and comprise a positive frequency part P and a negative frequency part N. Any imperfection is shown on the negative frequency part of the characteristic.

Taking Figure 6 as an example the effects of the mismatch in the resistance R3 are shown as a peak of increasing amplitude as the value of the resistance R3 is increased in 5% increments up to a maximum of 25%.

In Figure 7, the full line shows the peak due to a 5% error in the resistance R3 and in broken lines the effect of improvement obtained by the fine adjustment of the input phase. The dip in the broken line is due to the fact the errors are frequency dependent.

5 Figure 8 is a graph illustrating a lack of image rejection caused by increasing the value of the capacitance C6 shown in Figure 2 by 25% in steps of 5%.

Figure 9 is a graph illustrating by a full line a lack of image rejection caused by 5% error in capacitance C6 shown in Figure 2 improved by fine
10 adjustment of the input amplitude (broken lines).

Figure 10 is a graph illustrating the lack of image rejection caused by increasing the value of amplitude of a cross-coupling gyrator JC17 shown in Figure 2 by 25% in steps of 5%.

Figure 11 is a graph illustrating by a full line the lack of image rejection
15 caused by 5% error in amplitude of the cross-coupling gyrator JC17 shown in Figure 2 improved by fine adjustment of input amplitude (broken lines).

Figure 12 is a graph illustrating the lack of image rejection caused by a phase lead/lag of 5 degrees of the cross-coupling gyrator JC17 shown in Figure
2.

20 Finally, Figure 13 is a graph illustrating by a full line the lack of image rejection caused by a 5 degree error in phase of the cross-coupling gyrator JC17 shown in Figure 2 improved by fine adjustment of input phase (broken lines).

These mismatches are, in general, the most significant ones in terms of
25 the resultant lack of image rejection although the actual degree of mismatch used in these examples is much greater than would normally be expected in practice. They have been used solely to make the resultant lack of image rejection clear.

From reading the present disclosure, other modifications will be apparent
30 to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of phasing

receivers and component parts thereof and which may be used instead of or in addition to features already described herein.

Industrial Applicability

- 5 Phasing receivers, fabricated as integrated circuits, for use in telecommunications products.

CLAIMS

1. A phasing receiver having a polyphase filter in which lack of image rejection is improved by the fine adjustment of the phase and/or amplitude of input signals.
2. A phasing receiver comprising an input, first and second signal mixing means for providing quadrature related low IF frequencies, a polyphase filter having inputs coupled to outputs of the first and second signal mixing means and signal demodulating means coupled to outputs of the polyphase filter, and means for effecting fine adjustment of the phase and/or amplitude of signals applied to the inputs of the polyphase filter to compensate for less than optimum image rejection.
3. A phasing receiver as claimed in Claim 2, characterised in that the adjustment means is provided to adjust phase and/or amplitude of the input signals to at least one of the first and second signal mixing means.
4. A phasing receiver as claimed in Claim 2, characterised in that local oscillator signal generating means is coupled to the first and second signal mixing means, and in that the adjustment means comprise phase adjustment means provided in the local oscillator signal path.
5. A phasing receiver as claimed in Claim 2, characterised in that local oscillator signal generating means is coupled to the first and second signal mixing means, and in that the adjustment means comprise amplitude adjustment means provided in the local oscillator signal path.
6. A phasing receiver as claimed in Claim 2, characterised in that the adjustment means comprise amplitude adjustment means provided in a signal path to at least one input of the polyphase filter.

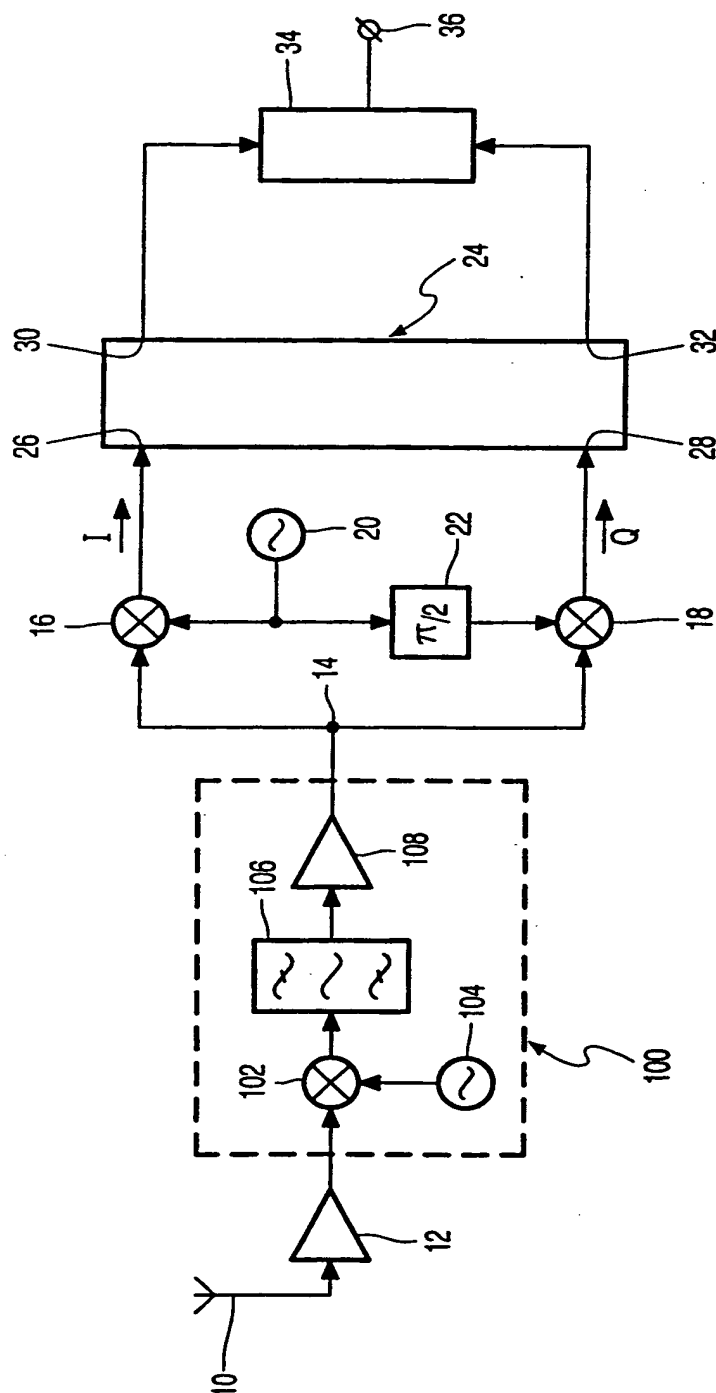
7. A phasing receiver as claimed in Claim 2, characterised in that the adjustment means comprise phase adjustment means provided in a signal path to at least one input of the polyphase filter.

5

8. A phasing receiver as claimed in any one of Claims 2 to 7, characterised in that the polyphase filter has N-stages, where N is an integer, and in that the phase adjustment means are provided to compensate for mismatches in an input stage.

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9. A phasing receiver as claimed in any one of Claims 1 to 8, fabricated as an integrated circuit.

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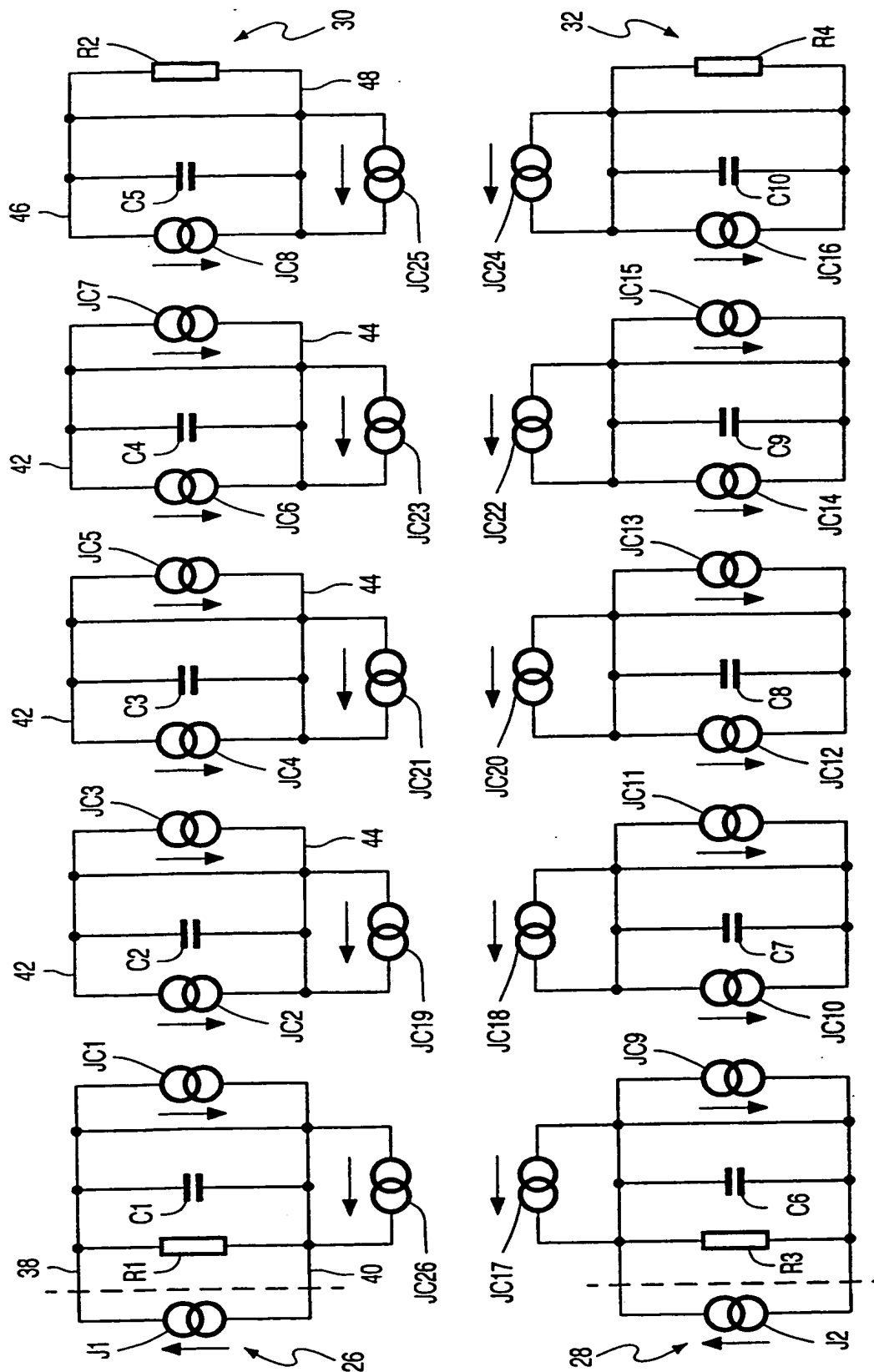


FIG. 2

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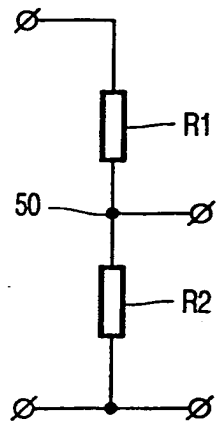


FIG. 3A

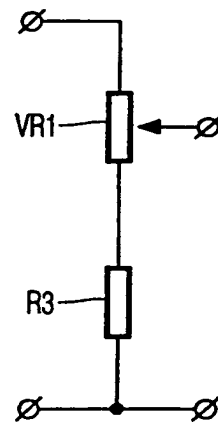


FIG. 3B

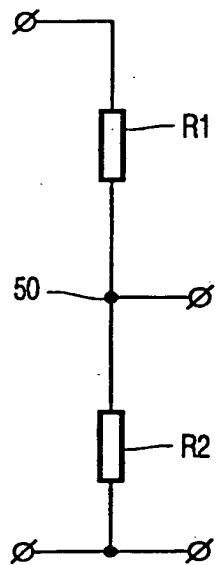


FIG. 4A

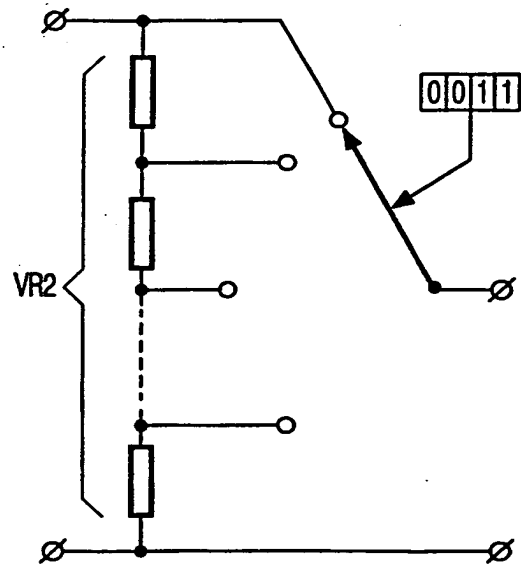


FIG. 4B

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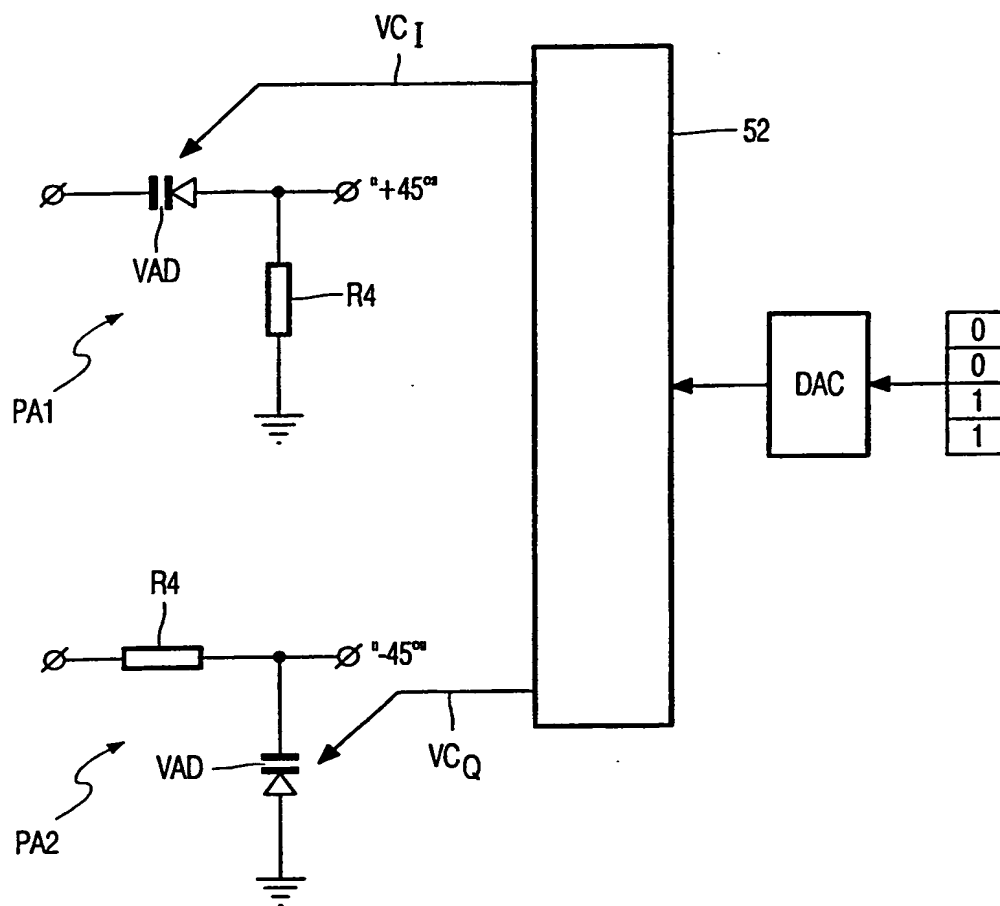


FIG. 5

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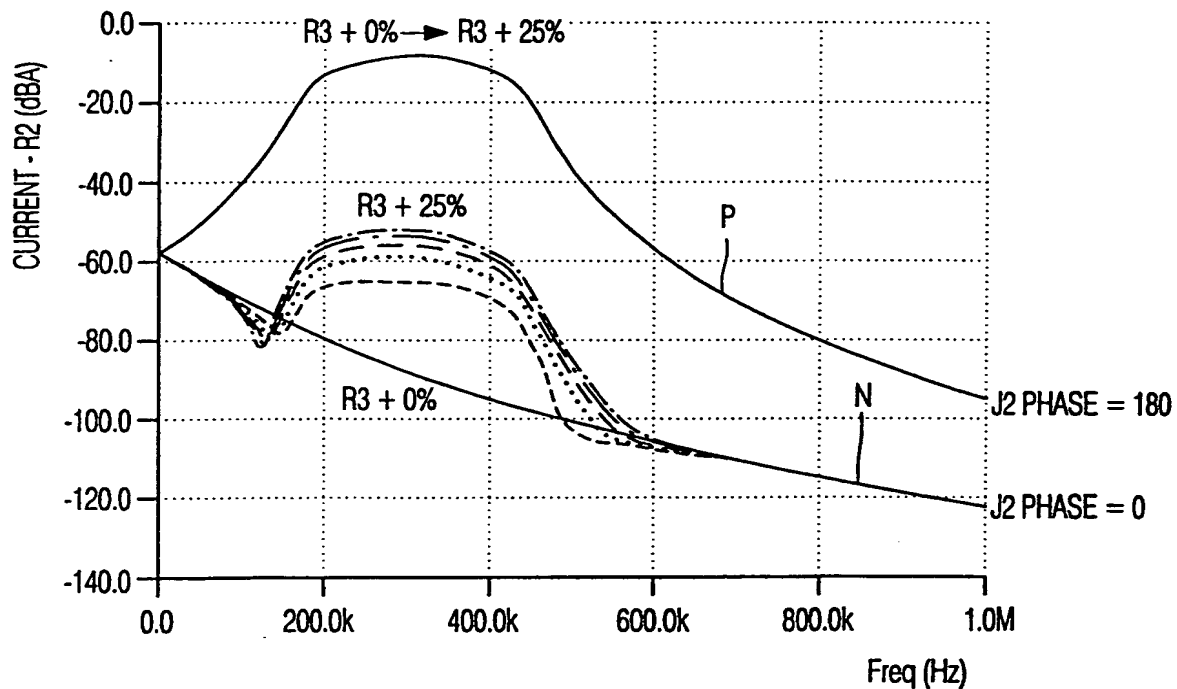


FIG. 6

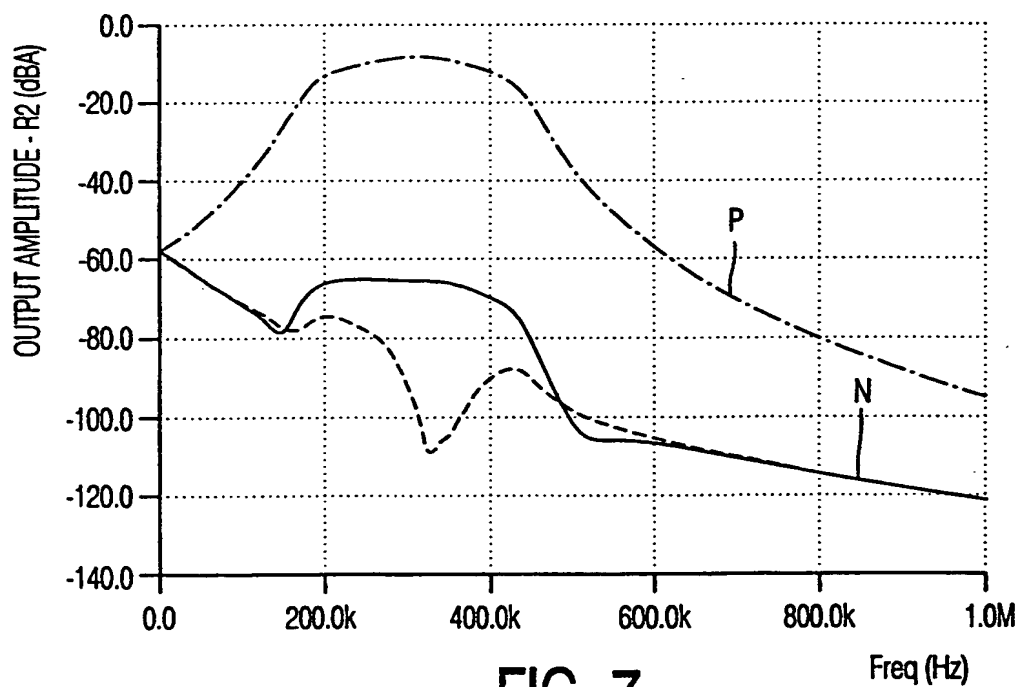


FIG. 7

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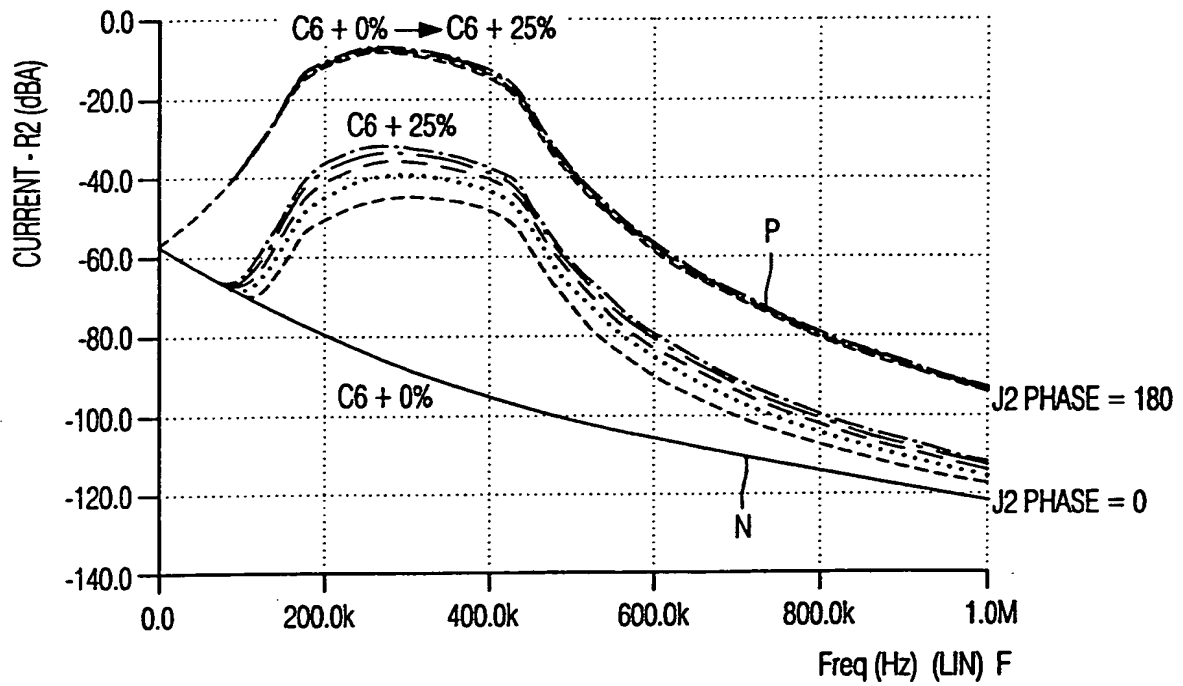


FIG. 8

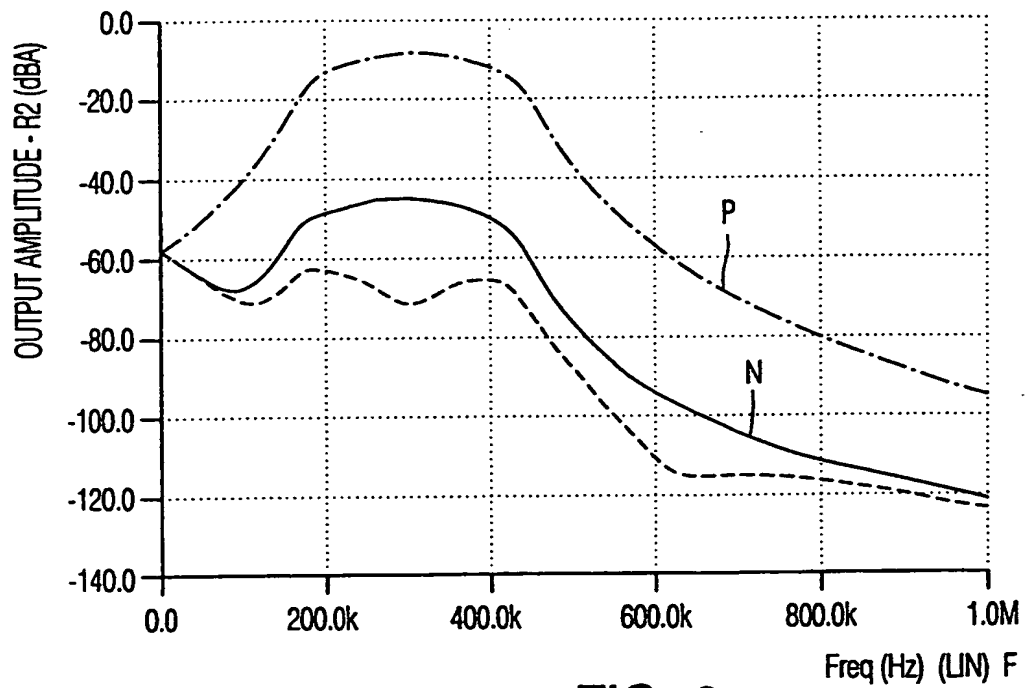


FIG. 9

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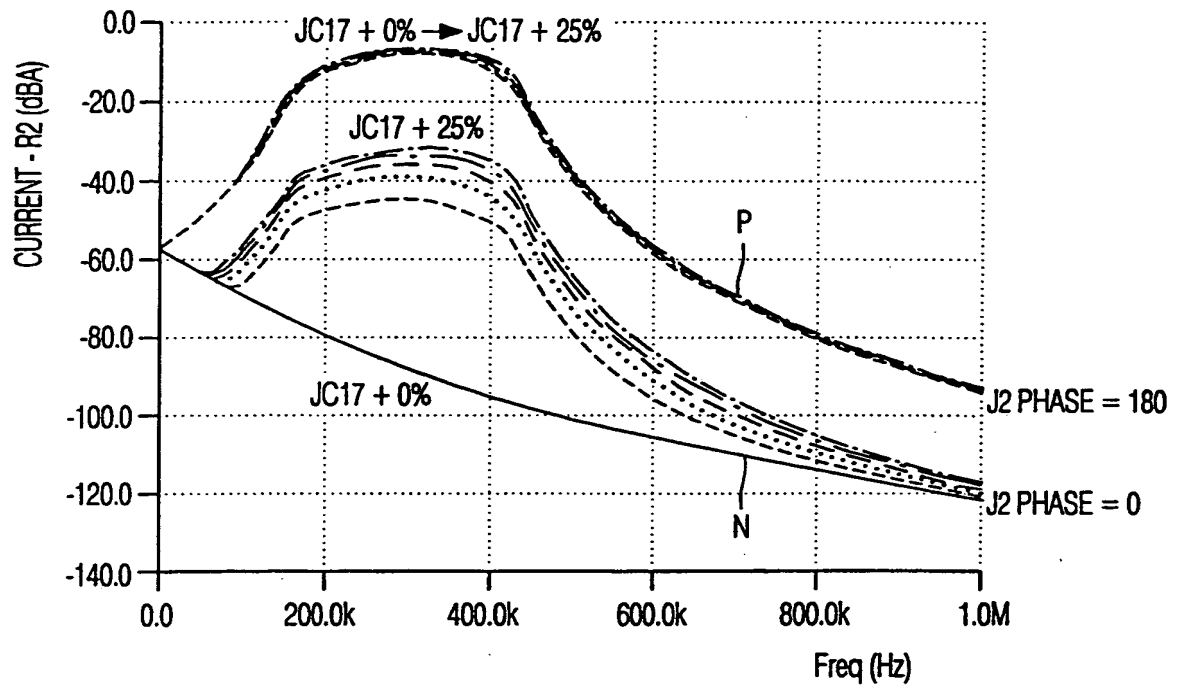


FIG. 10

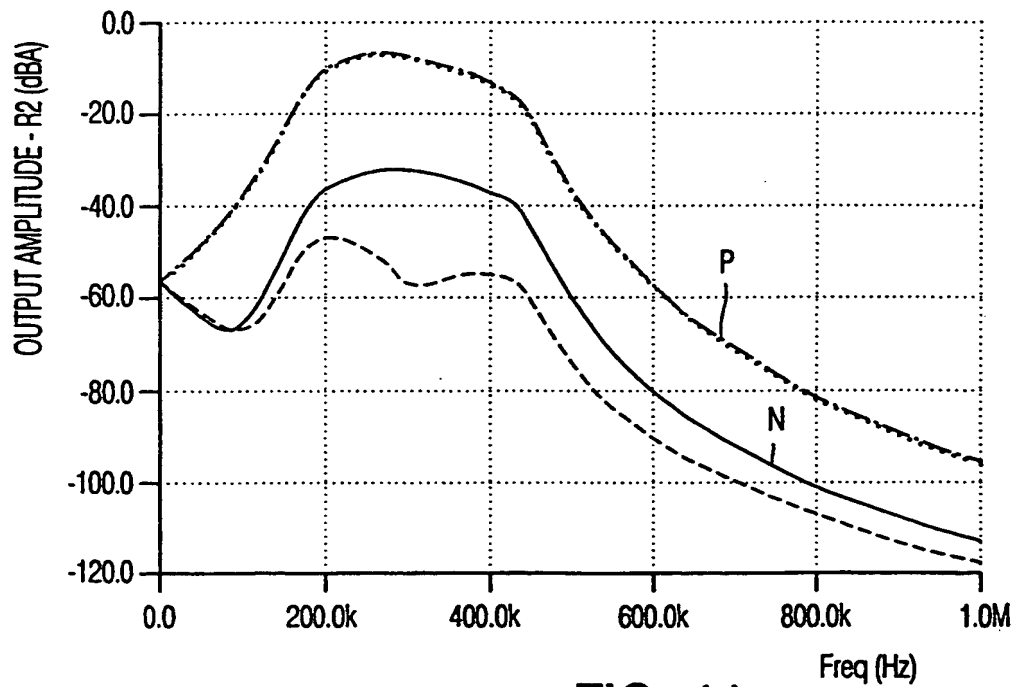


FIG. 11

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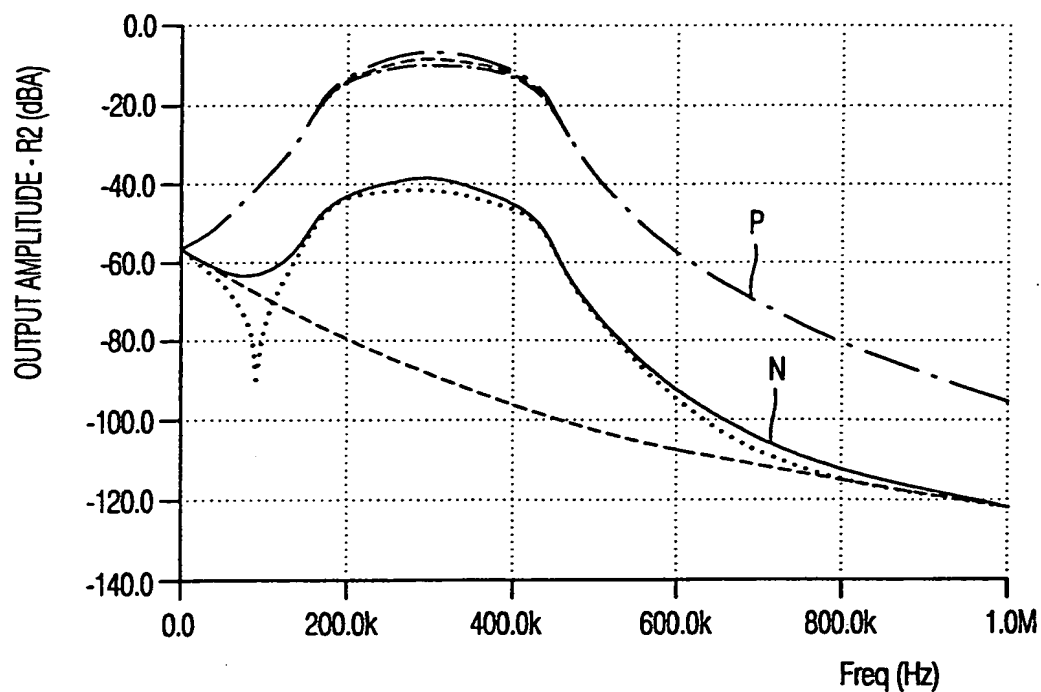


FIG. 12

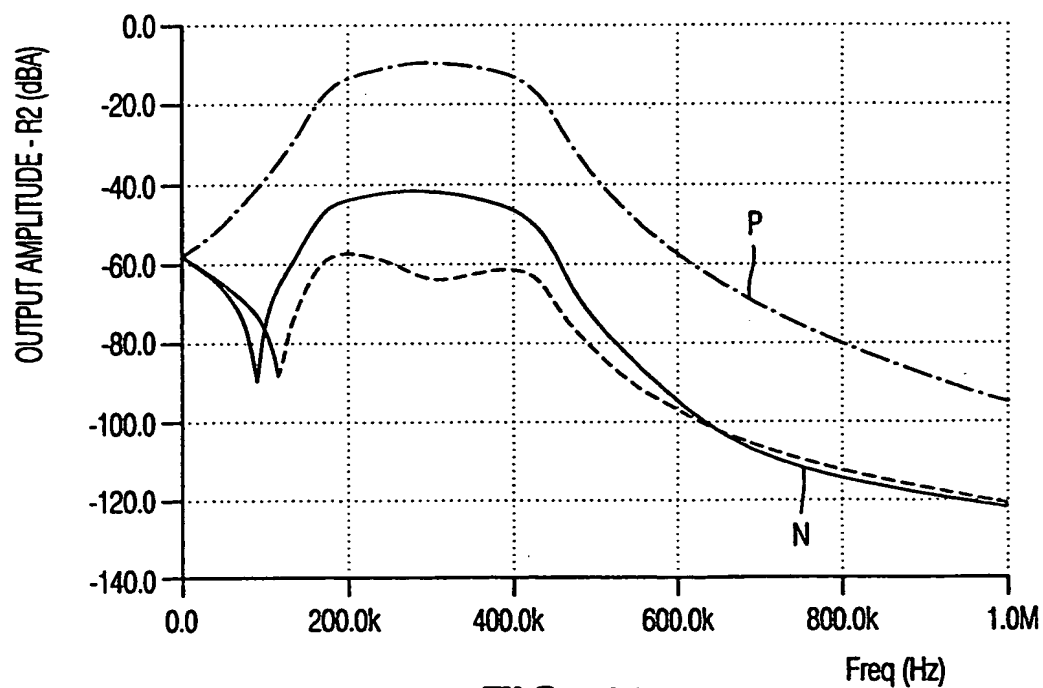


FIG. 13

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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant (for SE only): PHILIPS AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE).

(72) Inventors: MOORE, Paul, Anthony; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DAVIE, Alan, James; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

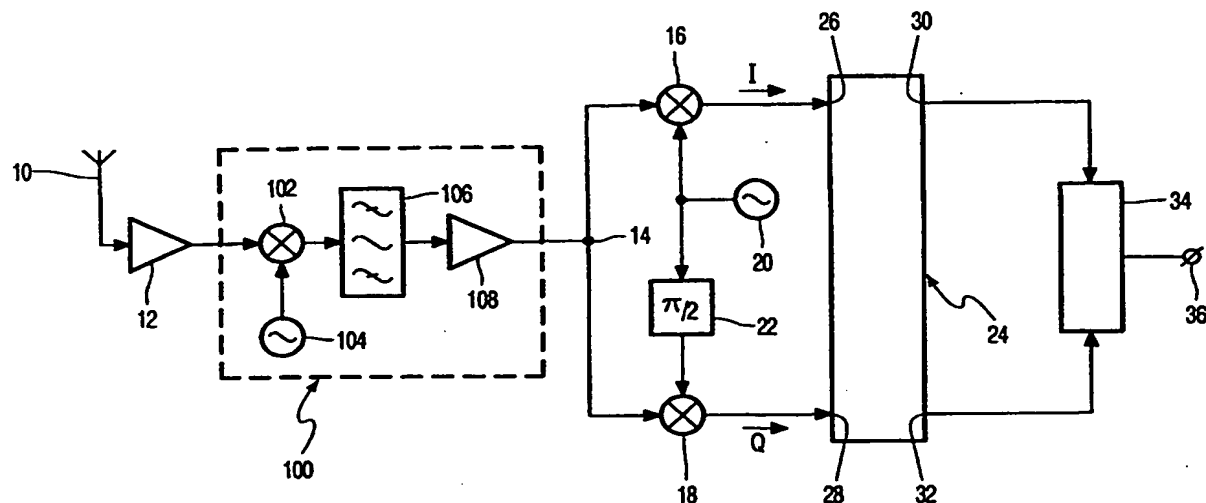
(74) Agent: MOODY, Colin, J.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).

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DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 98/01271

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04B 1/10, H04B 1/26, H03H 17/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04B, H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0576082 A1 (PHILIPS ELECTRONICS N.V.), 29 December 1993 (29.12.93), abstract --	1-9
A	US 4723318 A (CHRISTOPHER B. MARSHALL), 2 February 1988 (02.02.88), abstract --	1-9
A	EP 0344852 A1 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN), 6 December 1989 (06.12.89), abstract -- -----	1-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

7 April 1999

Date of mailing of the international search report

13 -04- 1999

Name and mailing address of the ISA/
Swedish Patent Office
Box 5055, S-102 42 STOCKHOLM
Facsimile No. +46 8 666 02 86

Authorized officer

Bengt Romedahl

Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/03/99

International application No.

PCT/IB 98/01271

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